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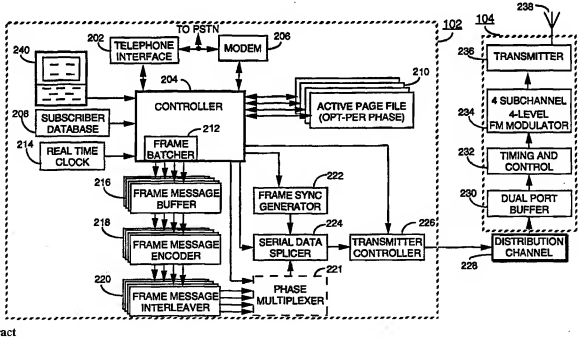

(57) Abstract

A communication system (100) broadcasting over a plurality of subchannels comprises a resource controller unit (204) having at least one of the plurality of subchannels serving as a control channel for addressing subscribers and directing them to receive messages or data on a set or a subset of the plurality of the subchannels, input means (240) for sending messages to the resource controller unit, and a selective call receiver (106) addressable by the resource controller unit, capable of receiving messages as directed by the resource controller on any of the subchannels and time slots directed by the resource controller.

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MULTIPLE SUBCHANNEL FLEXIBLE PROTOCOL METHOD AND APPARATUS

Technical Field

This invention relates generally to the field of communication systems and protocols and in particular, to a communication system and protocol that reallocates resources within multiple subchannels.

Background

There are many data communications systems in operation today which provide message distribution to data communication receivers, such as pagers. Many of these systems utilize signaling protocols which utilize time slots, or transmission frames, to which the pagers are assigned, thereby providing battery saving functions and other efficiencies during the normal course of message transmission. A paging terminal was provided in such systems to encode the received messages for transmission to the intended pagers during the assigned transmission frames. In signaling protocols such as the POCSAG signaling protocol, each time slot, or transmission frame, allowed for the transmission of only two code words, either both address code words, an address and a message code word, or two message code words. Since the transmission of even a simple telephone number required as a minimum two message code words, numeric message transmissions required on the average one and one-half frames, which periodically resulted in the inability to transmit address code words during the assigned transmission frames, because the transmission frame was filled by message code words associated with address code words transmitted in the previous transmission frame.

The above problem was alleviated in some signaling protocols by increasing the number of code words which could be transmitted in any transmission frame. However, when the number of transmittable code words is selected for the transmission frames, such transmission frames often have to be filled with idle code words when an insufficient number of messages have been received for transmission during any particular transmission frame. Such signaling protocols were also limited in the number of data communication receivers, or pagers, which could be assigned, or operated on any given channel, before the channel reached its maximum capacity. By increasing the transmission speed, additional pagers could be added to the system, however at the expense of a significant amount of unused channel capacity, until the system again filled up. Then, other systems resolved this problem (as described in pending applications assigned to the present assignee hereof and incorporated by reference herein by Schwendeman et al. having the Application No. 07/891,363 entitled "Data Communication Receiver Having Variable Length Message Carry-On" and by Kuznicki et al having the Application No. 07/891,503 and entitled "Data Communication Terminal Providing Variable Length Message Carry-On") by providing for a flexible system which enabled reconfiguring the amount of information which can be transmitted on the channel within the available transmission frames in order to maximize message throughput on a channel. These applications describe a flexible system which enables reconfiguring the amount of information which can be transmitted on a single channel within the available transmission frames. As the demand for greater capacity and throughput increases, there still exists a need for systems that make full use of subchannels to provide even greater throughput and flexibility than disclosed by the Applications by Kuznicki et al and Schwendeman et al. referred to herein above.

Summary of the Invention

A communication system broadcasting over a plurality of subchannels comprises a resource controller unit having at least

one of the plurality of subchannels serving as a control channel for addressing subscribers and directing them to receive messages or data on a set or a subset of the plurality of the subchannels, input means for sending messages to the resource controller unit, and a selective call receiver addressable by the resource controller unit, capable of receiving messages as directed by the resource controller on any of the subchannels and time slots directed by the resource controller.

In another aspect of the present invention, a method for receiving and decoding selective call messages transmitted in the form interleaved blocks of time divided signals on a plurality of subchannels to a plurality of selective call receivers, comprises the steps at one of the selective call receivers of decoding at least a first received block of information containing address and vector information for at least a first addressed message, at least a portion of the first received block being a control channel. Then, determining where the first addressed message will begin and the length of the first message from the address and vector information. And finally, decoding subsequent blocks of information on the plurality of subchannels to decode the first addressed message, the first addressed message being capable of residing in contiguous sections of blocks and portions of blocks on the plurality of subchannels.

Brief Description of the Drawings

FIG. 1 is an electrical block diagram of a data transmission system in accordance with the present invention.

FIG. 2 is an electrical block diagram of a terminal for processing and transmitting message information in accordance with the present invention.

FIGS. 3-5 are timing diagrams illustrating the transmission format of the signaling protocol utilized in accordance with the present invention.

FIGS. 6 and 7 are timing diagrams illustrating the synchronization signals utilized in accordance with the present invention.

FIG. 8 is an electrical block diagram of a data communication receiver in accordance with the present invention.

FIG. 9 is a more detailed electrical block diagram of the data communication receiver of FIG. 8 in accordance with the present invention.

FIG. 10 is an electrical block diagram of an alternative embodiment of a data communication receiver in accordance with the present invention.

FIG. 11 is a more detailed electrical block diagram of the data communication receiver of FIG. 10 in accordance with the present invention.

FIG. 12 is an electrical block diagram of yet another alternative embodiment of a data communication receiver in accordance with the present invention.

FIGs. 13-17 are diagrams illustrating the message capabilities of a system in accordance with the present invention.

Detailed Description of the Preferred Embodiment

FIG. 1 is an electrical block diagram of a data transmission system 100, such as a paging system, in accordance with the preferred embodiment of the present invention In such a data transmission system 100, messages originating either from a phone, as in a system providing numeric data transmission, or from a message entry device, such as an alphanumeric data terminal, are routed through the public switched telephone network (PSTN) to a paging terminal 102 which processes the numeric or alphanumeric message information for transmission by one or more transmitters 104 provided within the system. When multiple transmitters are utilized, the transmitters 104 preferably simulcast transmit the message information to data communication receivers 106. Processing of the numeric and alphanumeric information by the paging terminal 102, and the protocol utilized for the transmission of the messages is described below.

FIG. 2 is an electrical block diagram of the paging terminal 102 utilized for processing and controlling the transmission of the message information in accordance with the present invention. Short messages, such as tone-only and numeric messages which can be readily entered using a Touch-Tone telephone are coupled to the paging terminal 102 through a telephone interface 202 in a manner well known in the art. Longer messages, such as alphanumeric messages which require the use of a data entry device are coupled to the paging terminal 102 through a modem 206 using any of a number of well known modem transmission protocols. When a call to place a message is received, a controller 204 handles the processing of the message. The controller 204 is preferably a microcomputer, such as an MC68000 or equivalent, which is manufactured by Motorola Inc., and which runs various pre-programmed routines for controlling such terminal operations as voice prompts to direct the caller to enter the message, or the handshaking protocol to enable reception of messages from a data entry device. When a call is received, the controller 204 references information stored in the subscriber database 208 to determine how the message being received is to be processed. The subscriber data base 208 includes, but is not limited to such information as addresses assigned to the data communication receiver, message type associated with the address, and information related to the status of the data communication receiver, such as active or inactive for failure to pay the bill. A data entry terminal 240 is provided which couples to the controller 204, and which is used for such purposes as entry, updating and deleting of information stored in the subscriber data base 208, for monitoring system performance, and for obtaining such information as billing information.

The subscriber database 208 also includes such information as to what transmission frame and to what transmission phase the data communication receiver is assigned, as will be described in further detail below. The received message is stored in an active page file 210 which stores the messages in queue. Alternatively, the queue is provided in the active page file 210. The active page file 210 is preferably a dual

port, first in first out random access memory, although it will be appreciated that other random access memory devices, such as hard disk drives, can be utilized as well. Periodically the message information stored in each of the queue is recovered from the active page file 210 under control of controller 204 using timing information such as provided by a real time clock 214, or other suitable timing source. The recovered message information from the queue is sorted by frame number and is then organized by address, message information, and any other information required for transmission, and then batched into frames based upon message size by frame batching controller 212. The batched frame information is coupled to frame message buffers 216 which temporarily store the batched frame information until a time for further processing and transmission. Frames are batched in numeric sequence, so that while a current frame is being transmitted, the next frame to be transmitted is in the frame message buffer 216, and the next frame thereafter is being retrieved and batched. At the appropriate time, the batched frame information stored in the frame message buffer 216 is transferred to the frame encoder 218. The frame encoder 218 encodes the address and message information into address and message code words required for transmission, as will be described below. The encoded address and message code words are ordered into blocks and then coupled to a block interleaver 220 which interleaves preferably eight code words at a time for transmission in a manner well known in the art. The interleaved code words from each block interleaver 220 are then serially transferred on a bit by bit basis into a serial data stream by transmission phase. Optionally, if multiple phases are used, then the interleaved code words form each block interleaver 220 are then serially transferred to a phase multiplexer 221 (shown in ghost lines), which multiplexes the message information on a bit by bit basis into a serial data stream as before. The controller 204 next enables a frame sync generator 222 which generates the synchronization code which is transmitted at the start of each frame transmission. The synchronization code is multiplexed with address and message information under the control of controller

204 by serial data splicer 224, and generates therefrom a message stream which is properly formatted for transmission. The message stream is next coupled to a transmitter controller 226, which under the control of controller 204 transmits the message stream over a distribution channel 228. The distribution channel 228 may be any of a number of well known distribution channel types, such as wire line, an RF or microwave distribution channel, or a satellite distribution link. The distributed message stream is transferred to one or more transmitter stations 104, depending upon the size of the communication system. The message stream is first transferred into a dual port buffer 230 which temporarily stores the message stream prior to transmission. At an appropriate time determined by timing and control circuit 232, the message stream is recovered from the dual port buffer 230 and coupled to the input of preferably a 4 subchannel, 4-level FSK modulator 234. The modulated message stream is then coupled to the transmitter 236 for transmission via antenna 238.

FIGS. 3, 4 and 5 are timing diagrams illustrating the transmission format of the signaling protocol utilized in accordance with the preferred embodiment of the present invention. As shown in FIG. 3, the signaling protocol enables message transmission to data communication receivers, such as pagers, assigned to one or more of 128 frames which are labeled frame 0 through frame 127. It then will be appreciated that the actual number of frames provided within the signaling protocol can be greater or less than described above. The greater the number of frames utilized, the greater the battery life that may be provided to the data communication receivers operating within the system. The fewer the number of frames utilized, the more often messages can be queued and delivered to the data communication receivers assigned to any particular frame, thereby reducing the latency, or time required to deliver messages.

As shown in FIG. 4, the frames comprise a synchronization code (sync) followed preferably by eleven blocks of message information which are labeled block 0 through block 10. As

shown in FIG. 5. each block of message information comprises preferably eight address, control or data code words which are labeled word 0 through word 31 for each phase. Consequently, each phase in a frame allows the transmission of up to thirty-two (32) address, control and data code words. (In the case of 4 subchannel addressing, each phase in a frame allows the transmission of up to 4 times 32 words or 128 address, control and data code words. The address, control and data code words are preferably 31,21 BCH code words with an added thirty-second even parity bit which provides an extra bit of distance to the code word set. It will be appreciated that other code words, such as a 23,12 Golay code word could be utilized as well. Unlike the well known POCSAG signaling protocol which provides address and data code words which utilize the first code word bit to define the code word type, as either address or data, no such distinction is provided for the address and data code words in the signaling protocol utilized with the preferred embodiment of the present invention. Rather, address and data code words are defined by their position within the individual frames.

FIGS. 6 and 7 are timing diagrams illustrating the synchronization code utilized in accordance with the present invention. In particular, as shown in FIG. 6, the synchronization code comprises preferably three parts, a first synchronization code (sync 1), a frame information code word (frame info) and a second synchronization code (sync 2). As shown in FIG. 7, the first synchronization code comprises first and third portions, labeled bit sync 1 and BS1, which are alternating 1,0 bit patterns which provides bit synchronization, and second and fourth portions, labeled "A" and its complement "A bar", which provide frame synchronization. The second and fourth portions are preferably single 32,21 BCH code words which are predefined to provide high code word correlation reliability, and which are also used to indicate the data bit rate at which addresses and messages are transmitted. The table below defines the data bit rates which are used in conjunction with the signaling protocol.

Bit Rate	"A" Value
1600 bps	A1 and A1 bar
3200 bps	A2 and A2 bar
6400 bps	A3 and A3 bar
Not defined	A4 and A4 bar

As shown in the table above, three data bit rates are predefined for address and message transmission, although it will be appreciated that more or less data bit rates can be predefined as well, depending upon the system requirements. A fourth "A" value is also predefined for future use.

The frame information code word is preferably a single 32,21 BCH code word which includes within the data portion a predetermined number of bits reserved to identify the frame number, such as 7 bits encoded to define frame number 0 to frame number 127.

The structure of the second synchronization code is preferably similar to that of the first synchronization code described above. However, unlike the first synchronization code which is preferably transmitted at a fixed data symbol rate, such as 1600 bps (bits per second), the second synchronization code is transmitted at the data symbol rate at which the address and messages are to be transmitted in any given frame. Consequently, the second synchronization code allows the data communication receiver to obtain "fine" bit and frame synchronization at the frame transmission data bit rate.

In summary the signaling protocol utilized in accordance with an embodiment of the present invention comprises 128 frames which include a predetermined synchronization code followed by eleven data blocks which comprise eight address, control or message code words per phase. The synchronization code enables identification of the data transmission rate, and insures synchronization by the data communication receiver with the data code words transmitted at the various transmission rates.

The protocols described in the applications by Kuznicki et al and Schwendeman et al. are becoming known in the paging industry as the FLEX protocol. FLEX allows a communication

system to address and vector messages within a single channel, whereas the present invention allows a communication system to address and vector messages to one of N other subchannels in one embodiment, or in another embodiment, the communication system allows for the addressing and vectoring of messages to up to N subchannels simultaneously, where N can almost be any integer number . The following examples, for simplicity, illustrate embodiments where N=4, but of course, the scope of the claimed invention contemplates the embodiment where N can be any integer. For future reference, an embodiment where one of four subchannels can be addressed and vectored shall be called a 1X4 system, protocol, or receiver and an embodiment where four of four subchannels can be addressed and vectored simultaneously shall be called a 4X4 system, protocol, or receiver.

FIG. 8 is a block diagram of an embodiment of data communication receiver 106 in accordance with the present invention. The receiver 106 comprises of an antenna 802 coupled to a receiver module 804 which is coupled to a controller 816 via a 1X4 Decoder module 895 and a via synthesizer 899. The receiver 106 further includes memory 890 and input and output devices (885 & 880) as known in the art.

FIG. 9 is a more detailed electrical block diagram of the data communication receiver 106 shown in FIG. 8 in accordance with the present invention. The heart of the data communication receiver 106 is a controller 816, which is preferably implemented using an MC68HC11 microcomputer, such as manufactured by Motorola, Inc. The microcomputer controller, hereinafter called the controller 816, receives and processes inputs from a number of peripheral circuits, as shown in FIG. 9, and controls the operation and interaction of the peripheral circuits using software subroutines. The use of a microcomputer controller for processing and control functions is well known to one of ordinary skill in the art.

The data communication receiver 106 is capable of receiving address, control and message information, hereafter called "data" which is modulated using preferably 2-level and 4-

level frequency modulation techniques. The transmitted data is intercepted by an antenna 802 which couples to the input of a receiver section 804. Receiver section 804 processes the received data in a manner well known in the art, providing at the output an analog 4-level recovered data signal, hereafter called a recovered data signal. The recovered data signal is coupled to one input of a threshold level extraction circuit 808, and to an input of a 4-level decoder 810. The threshold level extraction preferably comprises two clocked level detector circuits (not shown) which have as inputs the recovered data signal. A level detector could detect the peak signal amplitude value and provide a high peak threshold signal which is proportional to the detected peak signal amplitude value, while another level detector detects the valley signal amplitude value and provides a valley threshold signal which is proportional to the detected valley signal amplitude value of the recovered data signal. Resistors are then utilized to enable decoding the 4-level data signals as will be described below.

When power is initially applied to the receiver portion, as when the data communication receiver is first turned on, a clock rate is preset to select a 128X clock, i.e. a clock having a frequency equivalent to 128 times the slowest data bit rate, which as described above is 1600 bps. The 128X clock is generated by 128X clock generator 844, as shown in FIG. 8, which is preferably a crystal controlled oscillator operating at 204.8 KHz (kilohertz). The output of the 128X clock generator 844 couples to an input of frequency divider 846 which divides the output frequency by two to generate a 64X clock at 102.4 KHz. The 128X clock allows the level detectors in the threshold level extraction circuit 808 to asynchronously detect in a very short period of time the peak and valley signal amplitude values, and to therefore generate the low (Lo), average (Avg) and high (Hi) threshold output signal values required for modulation decoding. After symbol synchronization is achieved with the synchronization signal, the controller 816 generates a second control signal to enable selection of a 1X symbol clock which is generated by symbol synchronizer 812 as shown in FIG. 9.

The most significant bit (MSB) output from the 4-level decoder 810 is coupled to an input of the symbol synchronizer 812 and provides a recovered data input generated by detecting the zero crossings in the 4-level recovered data signal. The symbol synchronizer 812 preferably uses the 64X clock at 102.4 KHz which is generated by frequency divider 846. A control signal (1600/3200) is provided to the symbol synchronizer 812 and is used to select the sample clock rate for symbol transmission rates of 1600 and 3200 symbols per second. The 1X and 2X symbol clocks are generated with 1600, 3200 and 6400 bits per second and are synchronized with the recovered data signal.

The 4-level binary converter 814 uses a 1X symbol clock and a 2X symbol clock along with the symbol output signals (MSB, LSB) and a selector signal (2L/4L) from the controller to select and provide control of the conversion of the symbol output signals as either 2-level FSK data, or 4-level FSK data. When the 2-level FSK data conversion (2L) is selected, only the MSB output is selected which is coupled to the input of a parallel to serial converter (not shown). When the 4-level FSK data conversion (4L) is selected, both the LSB and MSB outputs are selected which are coupled to the inputs of the parallel to serial converter.

Returning to FIG. 8, a serial binary data stream generated by the 4-level to binary converter 814 is coupled to inputs of a synchronization word correlator 818 and a demultiplexer 820. The synchronization word correlator has predetermined "A" word synchronization patterns that are recovered by the controller 816 from a code memory 822 and are coupled to an "A" word correlator (not shown). When the synchronization pattern received matches one of the predetermined "A" word synchronization patterns within an acceptable margin of error, an "A" or "A-bar" output is generated and is coupled to controller 816. The particular "A" or "A-bar" word synchronization pattern correlated provides frame synchronization to the start of the frame ID word, and also defines the data bit rate of the message to follow.

The serial binary data stream is also coupled to an input of the frame word decoder (not shown) which decodes the frame word and provides an indication of the frame number currently being received by the controller 816. During sync acquisition, such as following initial receiver turn-on, power is supplied to the receiver portion by battery saver circuit 848 which enables the reception of the "A" synchronization word, as described above, and which continues to be supplied to enable processing of the remainder of the synchronization code. The controller 816 compares the frame number currently being received with a list of assigned frame numbers stored in code memory 822. Should the currently received frame number differ from an assigned frame numbers, the controller 816 generates a battery saving signal which is coupled to an input of battery saver circuit 848, suspending the supply of power to the receiver portion. The supply of power will be suspended until the next frame assigned to the receiver, at which time a battery saver signal is generated by the controller 816 which is coupled to the battery saving circuit 848 to enable the supply of power to the receiver portion to enable reception of the assigned frame.

Returning to the operation of the synchronization correlator, a predetermined "C" word synchronization pattern is recovered by the controller 816 from a code memory 822 and is coupled to a "C" word correlator (not shown). When the synchronization pattern received matches the predetermined "C" word synchronization pattern with an acceptable margin of error, a "C" or "C-bar" output is generated which is coupled to controller 816. The particular "C" or "C-bar" synchronization word correlated provides "fine" frame synchronization to the start of the data portion of the frame. (See FIGs. 6 and 7).

The start of the actual data portion is established by the controller 816 generating a block start signal (Blk Start) which is coupled to inputs of a word de-interleaver 824.

Optionally, if multiple phases are used, then the block start signal is coupled to the inputs of a word de-interleaver 824 and a data recovery timing circuit 826. The block start signal is used to generate clocked phase signals which are synchronized with the

incoming message symbols. The clocked phase signal outputs of the phase timing generator 826 are coupled to inputs of a phase selector 828. During operation, the controller 816 recovers from the code memory 822, the transmission phase number to which the data communication receiver is assigned. The phase number is transferred to the phase select output (Ø Select) of the controller 816 and is coupled to an input of phase selector 828. A phase clock, corresponding to the transmission phase assigned, is provided at the output of the phase selector 828 and is coupled to clock inputs of the demultiplexer 820, block de-interleaver 824, and address and data decoders 830 and 832, respectively. The demultiplexer 820 is used to select the binary bits associated with the assigned transmission phase which are then coupled to the input of block de-interleaver 824, and clocked into the de-interleaver array on each corresponding phase clock.

The de-interleaver array is preferably a 32x32 bit array which de-interleaves thirty-two interleaved address, control or message code words, corresponding to one transmission block. The de-interleaved address code words are coupled to the input of address correlator 830. The controller 816 recovers the address patterns assigned to the data communication receiver, and couples the patterns to a second input of the address correlator. When any of the de-interleaved address code words matches any of the address patterns assigned to the data communication receiver within an acceptable margin of error, the message information associated with the address is then decoded by the data decoder 832 and stored in a message memory 850 in a manner well known to one of ordinary skill in the art. Following the storage of the message information, a sensible alert signal is generated by the controller 816. The sensible alert signal is preferably an audible alert signal, although it will be appreciated that other sensible alert signals, such as tactile alert signals, and visual alert signals can be generated as well. The audible alert signal is coupled by the controller 816 to an alert driver 834 which is used to drive an audible alerting device, such as a speaker or a transducer 836. The user can override the alert

signal generation through the use of user input controls 838 in a manner well known in the art.

Following the detection of an address associated with the data communication receiver, the message information is coupled to the input of data decoder 832 which decodes the encoded message information into preferably a BCD or ASCII format suitable for storage and subsequent display. The stored message information can be recalled by the user using the user input controls 838 whereupon the controller 816 recovers the message information from memory, and provides the message information to a display driver 840 for presentation on a display 842, such as an LCD display.

Referring to FIG. 10, another block diagram of an embodiment of the data communication receiver 106 in accordance with the present invention is shown. The receiver 106 comprises of an antenna 802 coupled to a receiver module 804 which is coupled to a controller 875 via a 4X4 Decoder module 897 and a via synthesizer 899. The receiver 106 further includes memory 890 and input and output devices (885 & 880) as known in the art. In one embodiment of the block diagram of FIG. 10, the receiver 106 would appear very much like the receiver of FIG. 9, except that the front end and decoder for the 4X4 FLEX receiver can appear as the block diagram shown in FIG. 11.

As before, the receiver 106 in FIG. 11 includes a receiver module 804 having an antenna 802. The receiver is coupled to a more sophisticated synthesizer 900 via a bank of mixers 310, 312, 314, and 316. The mixed signals from the bank of mixers is provided to the 4X4 decoder module 897. The module preferably comprises a bank of bandpass filters, detectors and decoders along with the appropriate amplification as is known in the art. Each bandpass filter (320, 322, 324 and 326 respectively) should be ideally designed to pass an appropriate subchannel on to their respective detectors (330, 332, 334, and 336) and their respective decoders (340, 342, 344, and 346). The signals from the decoder module 897 are then manipulated by the controller/data combiner in much the same manner as the controller 816 of FIG. 9. Of

course, the receiver 106 includes memory 890, and user input and output devices 885 and 880 respectively.

Referring to FIG. 12, another alternative embodiment is shown for the receiver 106 in FIG. 10 using a Digital Signal Processor (DSP) such as the Motorola DSP56001 or its functional equivalent. The receiver 106 of FIG. 12 preferably includes a linear receiver 404 having an antenna 402. Depending on the speed of the DSP, memory management and other housekeeping routines can be handled by the DSP. Otherwise, an optional controller 408, such as the controllers described in previous embodiments could be used. Ideally, in a 4X4 FLEX receiver, the DSP 406 will handle for four subchannels each: threshold level extraction, level synchronization, level synchronization correlation, data decoding, and data combining. Additionally, the DSP will also serve the functions of battery saving, de-multiplexing, de-interleaving, address correlation, phase selecting, and phase timing. Optionally, some of these tasks, and other tasks if needed, can be handled or shared by the controller 408. Finally, as usual, the receiver 106 includes memory 410, and user input and output devices 412 and 414 respectively.

FIGs. 13-17 illustrate typical timing diagrams associated with several embodiments in accordance with the present invention. FIG. 13 illustrates the timing diagram for a 1X4 FLEX receiver. The vector and addressing information will usually be found in the in the first subchannel, designated here as subchannel #0. Subchannel #0 or a portion of subchannel #0 will also be know as the control channel or the addressing channel. The vectoring information will usually designate what type of information will be received (suchas Hexidecimal or alphanumeric and whether the information will be provided on a single subchannel or on a multiple subchannel). The addressing information will designate what particular Word Number the message will start within the particular subchannel. In the case of a multiple subchannel message, the addressing information will designate what particular subchannel, block, and Word to begin providing the message. Additionally, the addressing can

designate corners in messages to provide further efficiency in messaging. Some of these features will become more apparent in the following discussions with regards to FIGS. 18-21.

Thus, in FIG. 13, the vectoring and addressing information in subchannel #0 directs the 1X4 Flex receiver to decode message #1 in subchannel 2 at a particular block and word. It should be understood that the 1X4 Flex receiver could have been directed to decode message #1 in any one of the available (four in this instance) subchannels, not just the subchannel shown. In FIG. 14, the vectoring and addressing information in subchannel #1 directs a 4X4 Flex receiver to decode the repeated message #1 in each of the subchannels at different blocks and words. Further note as illustrated in FIGs. 13 and 14, that it is within contemplation of the present invention that the control channel can reside on any of the subchannels (the intermediary subchannels and the highest or last subchannel), not just subchannel #0 (the lowest or first subchannel) as shown in FIG. 13.

In FIG. 15, the vectoring and addressing information in this case directs a Flex 4X4 receiver to decode three different sized messages (message #1, #2 and #3) at different subchannels. In the case of message #1, the message is decoded at a later time frame portion within subchannel #0. Message #2 is decoded in portions of contiguous "areas" within subchannels #1 and #2, while message #3 is decoded in portions of subchannel 3.

FIG. 16 is the same illustration as FIG. 15, but further illustrating the blocks and block boundaries preferably associated with the present invention. As shown, there are preferably 8 blocks within the block boundaries which are decoded at a time. The addressing and vectoring information in subchannel #0 first decoded by the 4X4 Flex receiver will direct the receiver to decode message #1 at the beginning at block 8 of subchannel #0, message #2 at the beginning of block 6 of subchannel #1 (and ending at block 10 of subchannel #2), and message #3 at the beginning of block 4 of subchannel 3.

Of course, the present invention maintains the flexibility found in the embodiments of Kuznicki et al and Schwendeman et

al in terms of being able to send and receive messages at variable speeds, but additionally, the present invention allows the receiver to send both 1X4 Flex messages and 4X4 Flex messages and further pack them within a 4 subchannel format that provides great efficiency as shown in FIG. 17. In this case, the receiver is shown as decoding messages in blocks of 5, where there are 11 blocks to a frame as previously described with regard to FIGs. 3-7. (Please note these are not the only formats available contemplated for use with the claimed invention.) When the receiver decodes the first five blocks (probably the last block of Frame N-1 and the first four blocks of Frame N), the receiver decodes the vectoring and addressing information first, found here in this case in the first block and portion of the second block of the second block of Frame N of subchannel #0. The vectoring information would indicate that the first four messages are 1X4 messages found in a single subchannel (subchannel #0), while the messages #5-#8 are 4X4 Flex messages decoded throughout portions of the four subchannels.

Operationally, a 1X4 FLEX receiver receiving message #4 (MSG4) as shown in FIG. 17, would decode block #0 and detect the message's address from the portion 2 of the block #0 and perhaps the message's vector from portion 3. Additionally, the receiver might decode block #1 and retrieve further vector information from portion 3. (Portion 1 of block #0 preferably contains Block Information Words). The 1X4 FLEX receiver would then decode blocks #2, #3 and #4 in sequence to extract its message.

Again referring to FIG. 17, a 4X4 FLEX receiver, receiving messages MSG5, MSG6, MSG7, and MSG8, would decode block #0 and block #1 to extract the address and vectors and then would decode the blocks from the start to end of the message based upon the vector information. This device would demodulate and decode data from multiple subchannels simultaneously as required based upon the subchannels used in transmission of the message.

A single device could decode all the messages in FIG. 17 in a variety of sized segments (for example, 5 blocks). The device

preferably has a receiver that decodes the addressing and vectoring information in blocks 1 and 2 in subchannel #0, then the message #3, along with portions of message #4 and portions of message #5, then message #1 along with more portions of message #4 and #5 and the beginning portions of message #6, then the remainder of message #2, with portions of message #4 and message #6 along with the remainder of message of #5. As the next segment of blocks are decoded, the remainder of messages #4 and #6 are decoded, and the entire message #7 is decoded. Additionally, a portion of message #8 is decoded. Finally, after the next segment of blocks are decoded, the remainder of message #8 is decoded by the receiver.

The 8 messages can be so efficiently packed together because of the flexibility of the protocol which allows for mixing of protocols and "corner" commands to make room for single subchannel messages (pages) among multiple subchannel messages or pages. These capabilities and advantages will become further apparent in the explanation of the format of the 32 (or more, actually 64 in the examples to follow) bit words used for vectoring and addressing the incoming messages at a receiver as shown in the tables below.

TABLE 1

HEX / Binary Vector (Single Subcarrier)

1 2 3 4 5 6 7 21	31	32
Information	Parity	Ck
x_0 x_1 x_2 x_3 V_0 V_1 V_2 V_3 b_0 b_1 b_2 b_3 b_4 b_5 b_6 b_7 b_8 y_0 y_1 m_0 s_0	p p p p p p p p p p	P
X_0 X_1 X_2 X_3 n_0 n_1 n_2 n_3 n_4 n_5 n_6 n_7 n_8 s_7 s_6 s_5 s_4 s_3 s_2 s_1 s_0	p p p p p p p p p p	P

V - Vector Type $V_3V_2V_1V_0$ = 0110 - HEX Vector Single Subcarrier
b - Word Number of message start $b_8b_7b_6b_5b_4b_3b_2b_1b_0$ (1 - 511 Decimal)
y - Subchannel assigned
m - 0 implies message is in this frame
1 implies message in future frame. s_7 - s_1 contains the frame num.
n - Number of message words $n_8n_7n_6n_5n_4n_3n_2n_1n_0$ (1 to 511 Decimal)
s - Spares
x - Std 4 bit Check Character

Table 1 shows the formatting for a HEX/Binary message using a 1X4 Flex format, which requires the designation of a vector type (HEX vector, single subchannel), the Word number where the message will start, the number of message words in the particular frame, and the subchannel assigned.

TABLE 2

HEX / Binary Vector (Multiple Subcarrier)

1 2 3 4 5 6 7 21	31	32
Information	Parity	Ck
$x_0\ x_1\ x_2\ x_3\ V_0\ V_1\ V_2\ V_3\ b_0\ b_1\ b_2\ b_3\ b_4\ b_5\ b_6\ b_7\ b_8\ b_9\ b_{10}\ d_0 d_1$	p p p p p p p p p p	p
$x_0\ x_1\ x_2\ x_3\ n_0\ n_1\ n_2\ n_3\ m_0\ c_0\ c_1\ c_2\ c_3\ c_4\ c_5\ e_0\ e_1\ e_2\ e_3\ e_4\ e_5$	p p p p p p p p p p	p

V - Vector Type $V_3V_2V_1V_0$ = 1110 - HEX Vector Multiple Subcarrier
b - Word of message start = $b_{10}b_9$-Subchannel, $b_8b_7b_6b_5$-Block, $b_4b_3b_2b_1b_0$-Word
d - Number of additional corners in message field (6 bits/corner)
n - Number of message words = $n_{10}n_9n_8n_7n_6n_5n_4n_3n_2n_1n_0$ (1 to 511 Decimal)
n_{10} - n_4 are in message field.
m - 0 implies message is in this frame
1 implies message is in future frame. c_0-e_0 represent the frame num.
The first corner information is in message field.
c - first Corner = c_5c_4-Subchannel, $c_3c_2c_1c_0$- Block
e - second Corner = e_5e_4-Subchannel, $e_3e_2e_1e_0$- Block
x - Std 4 bit Check Character

Table 2 illustrates the formatting for a HEX/Binary message using the 4X4 Flex format, which requires the designation of a vector type (HEX/Binary, multiple subchannel), the location where the first Word of the message will begin including information detailing the subchannel, block, and specific Word within the block where the message will begin, the number of message words, and cornering information which further defines within a frame and block of information where a particular message will reside when it is decoded by the receiver. The cornering information, as in the message start information, should include the subchannel location, block location, and in some cases the Word location. Note that there may be other more precise or more flexible methods within the scope and spirit of the present

invention than using "corner" commands , but "corner" commands are an efficient compromise

TABLE 3

Alphanumeric Vector (Single Subchannel)

1 2 3 4 5 6 7 21	31	32
Information	Parity	Ck
x_0 x_1 x_2 x_3 V_0 V_1 V_2 V_3 b_0 b_1 b_2 b_3 b_4 b_5 b_6 b_7 b_8 y_0 y_1 m_0 s_0	p p p p p p p p p p	P
x_0 x_1 x_2 x_3 n_0 n_1 n_2 n_3 n_4 n_5 n_6 n_7 n_8 s_7 s_6 s_5 s_4 s_3 s_2 s_1 s_0	p p p p p p p p p p	P

V - Vector Type $V_3V_2V_1V_0$ = 0101 - Alpha Vector Single Subcarrier
b - Word Number of message start $b_8b_7b_6b_5b_4b_3b_2b_1b_0$ (1 - 511 Decimal)
y - Subchannel assigned
m - 0 implies message is in this frame
1 implies message in future frame. s_7 - s_1 contains the frame number.
n - Num. of message words in this frame $n_8n_7n_6n_5n_4n_3n_2n_1n_0$ (1 to 511 Decimal)
s - Spares
x - Std 4 bit Check Character

Table 3 shows the formatting for a alphanumeric message using a 1X4 Flex format, which requires the designation of a vector type (alphanumeric, single subchannel), the Word number where the message will start, the number of message words in the particular frame, and the subchannel assigned.

TABLE 4

Alphanumeric Vector (Multiple Subchannel)

1 2 3 4 5 6 7 21	31	32
Information	Parity	Ck
x_0 x_1 x_2 x_3 V_0 V_1 V_2 V_3 b_0 b_1 b_2 b_3 b_4 b_5 b_6 b_7 b_8 b_9 b_{10} d_0 d_1	p p p p p p p p p p	P
x_0 x_1 x_2 x_3 n_0 n_1 n_2 n_3 m_0 c_0 c_1 c_2 c_3 c_4 c_5 e_0 e_1 e_2 e_3 e_4 e_5	p p p p p p p p p p	P

V - Vector Type $V_3V_2V_1V_0$ = 1101 - HEX Vector Multiple Subcarrier
b - Word of message start = $b_{10}b_9$-Subchannel, $b_8b_7b_6b_5$-Block, $b_4b_3b_2b_1b_0$- Word
d - Number of additional corners in message field (6 bits/corner)
n - Number of message words = $n_{10}n_9n_8n_7n_6n_5n_4n_3n_2n_1n_0$ (1 to 511 Decimal)
n_{10} - n_4 are in message field.
m - 0 implies message is in this frame
1 implies message is in future frame. c_0-e_0 represent the frame num.
The first corner information is in message field.
c - 1st Corner = c_5c_4-Subchannel, $c_3c_2c_1c_0$- Block
e - 2nd Corner = e_5e_4-Subchannel, $e_3e_2e_1e_0$- Block
x - Std 4 bit Check Character

Table 4 illustrates the formatting for an alphanumeric message using the 4X4 Flex format, which requires the designation of a vector type (alphanumeric, multiple subchannel), the location where the first Word of the message will begin including information detailing the subchannel, block, and specific Word within the block where the message will begin, the number of message words, and cornering information which as before, further defines within a frame and block of information where a particular message will reside when it is decoded by the receiver.

The present invention has been described in detail in connection with the disclosed embodiments. These embodiments, however, are merely examples and the invention is not restricted thereto. It will be understood by those skilled in the art that variations and modifications can be made within the scope and spirit of the present invention as defined by the appended claims.

What is claimed is:

Claims

1. A communication system broadcasting over a plurality of subchannels, comprising:

a resource controller unit having at least one of the plurality of subchannels serving as a control channel for addressing subscribers and directing them to receive messages or data on a set or a subset of the plurality of the subchannels;

input means for sending messages to the resource controller unit; and

a selective call receiver addressable by the resource controller unit, capable of receiving messages as directed by the resource controller on any of the subchannels and time slots directed by the resource controller.

2. The communication system of claim 1 wherein the control channel further addresses and directs subscribers to receive messages or data on a given time slot within a TDD frame and within a set or subset of the plurality of subchannels or within a portion of one of the plurality of subchannels.

3. A terminal in a communication system broadcasting over a plurality of subchannels, comprising:

a resource controller unit having at least one of the plurality of subchannels serving as a control channel for addressing subscribers and directing them to receive messages or data on a set or a subset of the plurality of the subchannels;

input means for sending messages to the resource controller unit; and

a transmitter for addressing a selective call receiver addressable by the resource controller unit, capable of receiving messages as directed by the resource controller on any of the subchannels and time slots directed by the resource controller.

4. The terminal of claim 3, wherein the control channel resides within a portion of the lowest or first subchannel and is used to address and vector messages to the remaining portion of the lowest subchannel and to the other subchannels.

5. A selective call receiver capable of receiving messages broadcast over a plurality of subchannels, comprising:

a receiver module capable of receiving selective call signals on the plurality of subchannels and providing a received signal;

a decoder module coupled to the receiver module;

a bank of mixers for mixing the received signal from the receiver module with an injection signal from a synthesizer to provide a mixed signal to the decoder module, the decoder module comprising of a corresponding bank of bandpass filters, detectors and decoders for each of the plurality of subchannels; and

a controller for controlling the decoder module, the synthesizer, a sensory alert device, and a display device all coupled to the controller.

6. A selective call receiver capable of receiving messages broadcast over a plurality of subchannels, comprising:

a receiver module capable of receiving selective call signals on the plurality of subchannels and providing a received signal;

a digital signal processor coupled to the receiver module for providing the function for each subchannel of threshold level extraction, level synchronization, level synchronization correlation, data decoding, and data combining and for providing the general functions of battery saving, de-multiplexing, de-interleaving, address correlation, phase selecting, and phase timing.

7. A method for queuing messages for transmission in a data communication terminal having an input for receiving messages and for assigning the same into a plurality of transmission frames and subchannels assigned for transmission to a plurality of data communication receivers, said method comprising the steps of:

storing the received messages in a first memory area;

generating periodic timing signals;

recovering the stored messages from the first memory in response to the periodic timing signals being generated;

queuing the recovered messages for the assigned transmission frame and subchannel into a second memory area having a predetermined queue capacity;

monitoring the second memory queue capacity, and expected queue capacities for one or more subsequent transmission frames and subchannels;

determining when the messages stored within the second memory area exceed the predetermined queue capacity;

storing the excess messages recovered in a third memory area;

generating designating information designating one or more subsequent transmission frames and subchannels during which the excess messages stored in the third memory area are to be transmitted; and

transmitting the messages and designating information stored in the second memory area within the assigned transmission frame and subchannel; and

transmitting the excess messages stored in the third memory area within the one or more subsequent transmission frames designated by the designating information.

8. A method for receiving and decoding selective call messages transmitted in the form of interleaved blocks of time divided signals on a plurality of subchannels to a plurality of selective call receivers, comprising the steps at one of the selective call receivers:

decoding at least a first received block of information containing address and vector information for at least a first addressed message, at least a portion of the first received block being a control channel;

determining where the first addressed message will begin and the length of the first message from the address and vector information; and

decoding subsequent blocks of information on the plurality of subchannels to decode the first addressed message, the first addressed message being capable of residing in contiguous sections of blocks and portions of blocks on the plurality of subchannels.

9. The method for receiving and decoding selective call messages of claim 8, wherein the step of decoding subsequent blocks of information further comprises the step of:

simultaneously demodulating and decoding information on the plurality of subchannels as directed by the address and vector information.

10. The method of claim 8, wherein the address and vector information contains start addresses and message lengths for a plurality of messages, wherein the plurality of messages can span a plurality of subchannels and a plurality of blocks within a time frame.

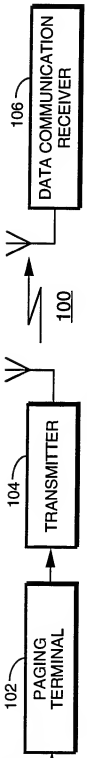
TO PSTN
102
PAGING TERMINAL
104
TRANSMITTER
100
106
DATA COMMUNICATION RECEIVER

FIG. 1

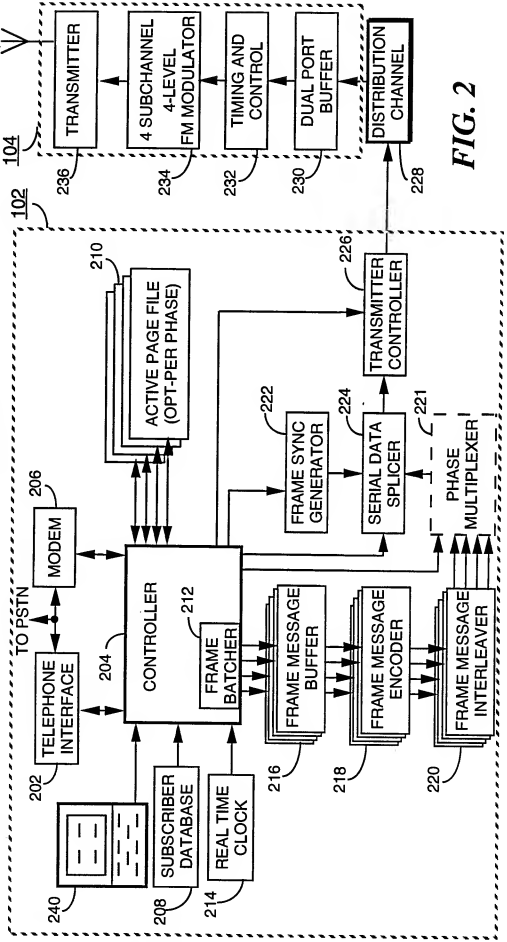
102
104
238
TRANSMITTER
236
4 SUBCHANNEL 4-LEVEL FM MODULATOR
234
TIMING AND CONTROL
232
DUAL PORT BUFFER
230
DISTRIBUTION CHANNEL
228
210
ACTIVE PAGE FILE (OPT-PER PHASE)
226
TRANSMITTER CONTROLLER
222
FRAME SYNC GENERATOR
224
SERIAL DATA SPLICER
221
PHASE MULTIPLEXER
206
MODEM
TO PSTN
204
CONTROLLER
212
FRAME BATCHER
TELEPHONE INTERFACE
202
FRAME MESSAGE BUFFER
216
FRAME MESSAGE ENCODER
218
FRAME MESSAGE INTERLEAVER
220
SUBSCRIBER DATABASE
208
REAL TIME CLOCK
214
240

FIG. 2

FIG. 3

FIG. 4

FIG. 5

FIG. 6

FIG. 7

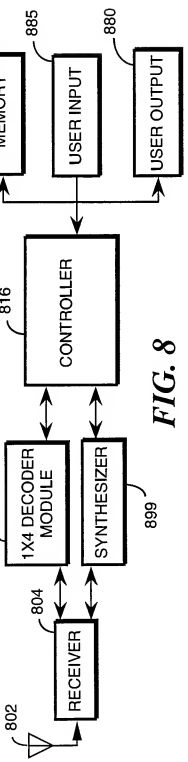
890
MEMORY
885
USER INPUT
880
USER OUTPUT
106
816
CONTROLLER
895
1X4 DECODER MODULE
899
SYNTHESIZER
804
RECEIVER
802

FIG. 8

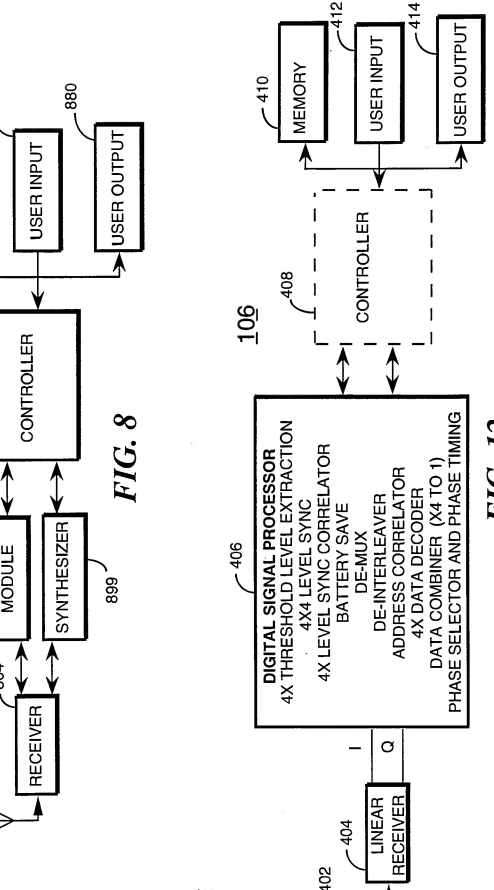
410
MEMORY
412
USER INPUT
414
USER OUTPUT
106
408
CONTROLLER
406
DIGITAL SIGNAL PROCESSOR
4X THRESHOLD LEVEL EXTRACTION
4X4 LEVEL SYNC
4X LEVEL SYNC CORRELATOR
BATTERY SAVE
DE-MUX
DE-INTERLEAVER
ADDRESS CORRELATOR
4X DATA DECODER
DATA COMBINER (X4 TO 1)
PHASE SELECTOR AND PHASE TIMING
I
Q
404
LINEAR RECEIVER
402

FIG. 12

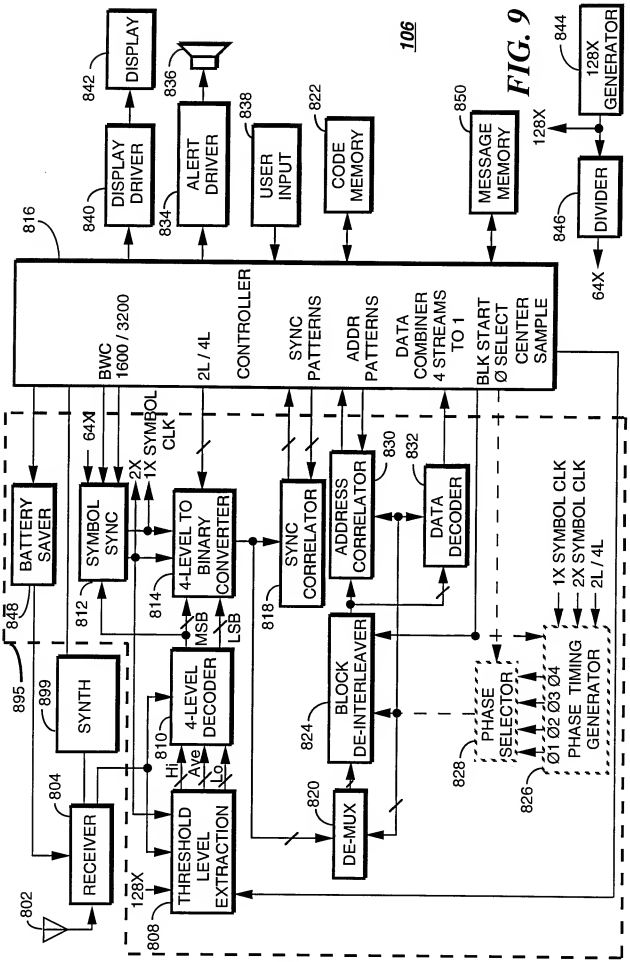
106
802
804
RECEIVER
128X
808
THRESHOLD LEVEL EXTRACTION
Hi
Ave
Lo
810
4-LEVEL DECODER
MSB
LSB
812
814
4-LEVEL TO BINARY CONVERTER
64X
2X
1X SYMBOL CLK
SYMBOL SYNC
848
BATTERY SAVER
895
899
SYNTH
820
DE-MUX
824
BLOCK DE-INTERLEAVER
818
SYNC CORRELATOR
830
ADDRESS CORRELATOR
832
DATA DECODER
828
PHASE SELECTOR
Ø1 Ø2 Ø3 Ø4
826
PHASE TIMING GENERATOR
1X SYMBOL CLK
2X SYMBOL CLK
2L / 4L
816
CONTROLLER
BWC 1600 / 3200
2L / 4L
SYNC PATTERNS
ADDR PATTERNS
DATA COMBINER 4 STREAMS TO 1
BLK START Ø SELECT CENTER SAMPLE
840
DISPLAY DRIVER
842
DISPLAY
834
ALERT DRIVER
836
838
USER INPUT
822
CODE MEMORY
850
MESSAGE MEMORY
128X
844
128X GENERATOR
846
DIVIDER
64X

FIG. 9

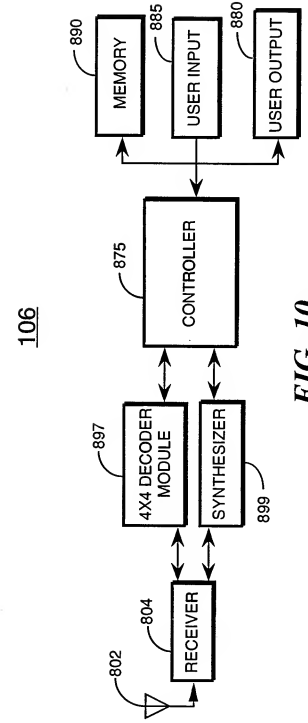
106
802
804
RECEIVER
897
4X4 DECODER MODULE
899
SYNTHESIZER
875
CONTROLLER
890
MEMORY
885
USER INPUT
880
USER OUTPUT

FIG. 10

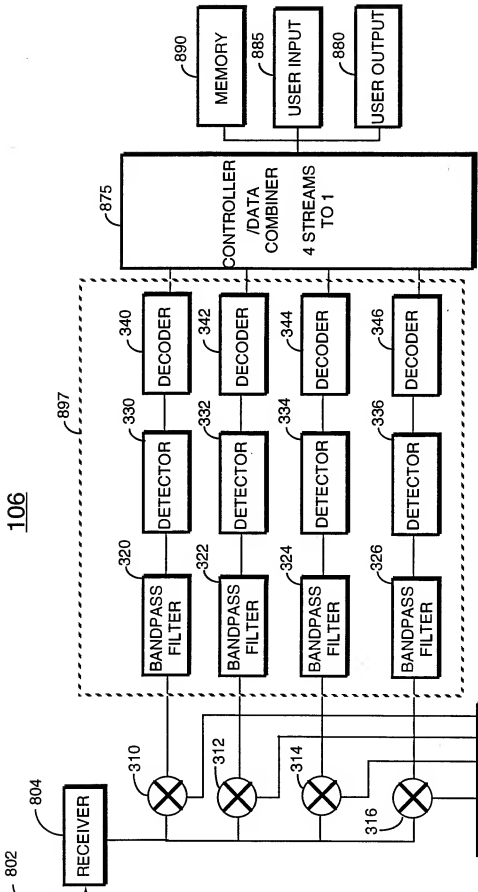
106
802
804
RECEIVER
310
312
314
316
SYNTHESIZER
900
897
320
322
324
326
BANDPASS FILTER
330
332
334
336
DETECTOR
340
342
344
346
DECODER
875
CONTROLLER /DATA COMBINER
4 STREAMS TO 1
890
MEMORY
885
USER INPUT
880
USER OUTPUT

FIG. 11

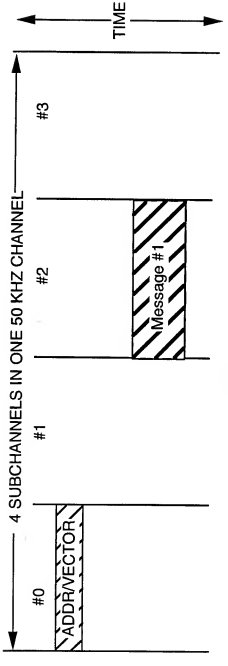
4 SUBCHANNELS IN ONE 50 KHZ CHANNEL
#0
#1
#2
#3
TIME
ADDR/VECTOR
Message #1

FIG. 13

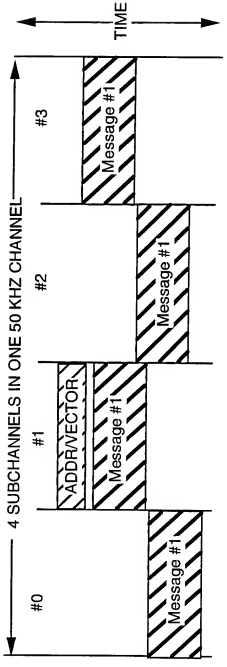
4 SUBCHANNELS IN ONE 50 KHZ CHANNEL
#0
#1
#2
#3
TIME
ADDR/VECTOR
Message #1

FIG. 14

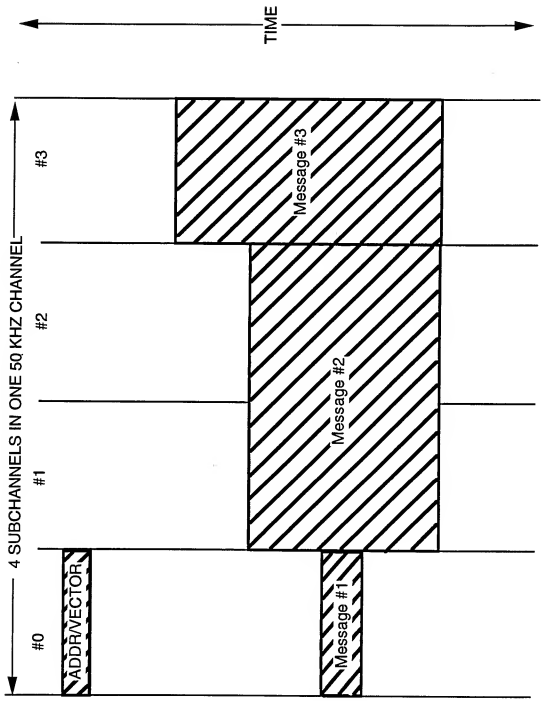
TIME
4 SUBCHANNELS IN ONE 50 KHZ CHANNEL
#0
#1
#2
#3
ADDR/VECTOR
Message #1
Message #2
Message #3

FIG. 15

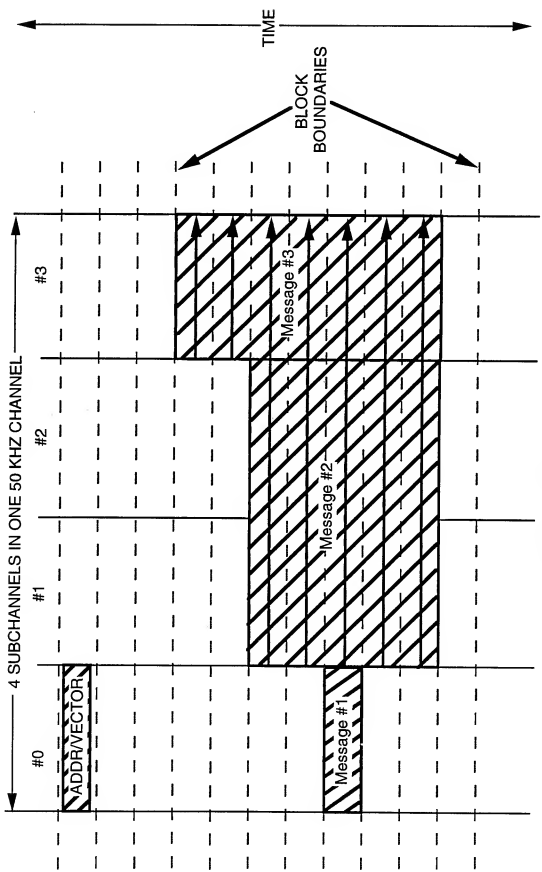
TIME
BLOCK BOUNDARIES
4 SUBCHANNELS IN ONE 50 KHZ CHANNEL
#0
#1
#2
#3
ADDR/VECTOR
Message #1
Message #2
Message #3

FIG. 16

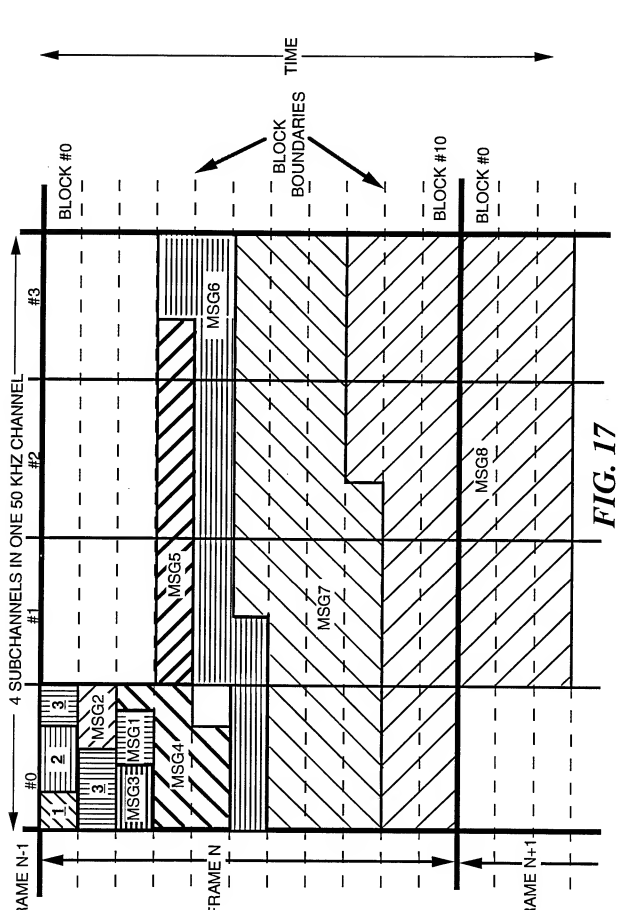
FRAME N-1
FRAME N
FRAME N+1
4 SUBCHANNELS IN ONE 50 KHZ CHANNEL
#0
#1
#2
#3
TIME
BLOCK BOUNDARIES
BLOCK #0
BLOCK #10
BLOCK #0
MSG1
MSG2
MSG3
MSG4
MSG5
MSG6
MSG7
MSG8
1
2
3
3

FIG. 17

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US95/05377

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H04Q 7/00
US CL :340/825.44; 379/57; 370/95.1
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 340/825.44; 379/57, 58, 60, 62; 370/94.1, 95.1

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US, A, 4,903,320 (HANAWA) 20 FEBRUARY 1990, COL. 1 LINES 27-46.	1-22
Y	US, A, 4,949,395 (RYDBECK) 14 AUGUST 1990, ABSTRACT, COL. 1 LINE 19 - COL. 2 LINE 19.	1-22
A	US, A, 5,278,890 (BEESON, JR. ET AL) 11 JANUARY 1994, ABSTRACT.	1
A	US, A, 5,260,944 (TOMABECHI) 09 NOVEMBER 1993, ABSTRACT.	1
A	US, A, 5,199,031 (DAHLIN) 30 MAY 1993, ABSTRACT.	1

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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